

Inductively Coupled Plasma etching of amorphous silicon nanostructures over nanotopography using C_4F_8/SF_6 chemistry

Harvey-Collard, Patrick,^{1,*} Jaouad, Abdelatif,² Drouin, Dominique,² and Pioro-Ladrière, Michel¹

¹*Département de physique, Université de Sherbrooke, Sherbrooke, QC, J1K 2R1, Canada*

²*Département de génie électrique et de génie informatique,
Université de Sherbrooke, Sherbrooke, QC, J1K 2R1, Canada*

(Dated: September 20th, 2012)

Inductively Coupled Plasma (ICP) etching of amorphous silicon (a-Si) nanostructures using a continuous C_4F_8/SF_6 plasma over nanotopography in silicon dioxide (SiO_2) is investigated. The coil power of the ICP system is used to tune the a-Si etch rate from 20 to 125 nm/min. The etch rates of a-Si, SiO_2 and electroresist are measured depending on the SF_6 ratio, platen power and chamber pressure and used to optimize the a-Si: SiO_2 etch selectivity. The results on nanostructures show that the presence of an insulating etch-stop layer affects the passivation ratio required to achieve vertical sidewalls. A low pressure is also necessary in order to etch the silicon nanostructure embedded into the oxide nanotrenches to form a highly conformable a-Si nanowire. We argue that both of these behaviors could be explained by surface charging effects. Finally, etching of 20 nm a-Si nanowires that cross 15 nm trenches in oxide with vertical sidewalls and a 4.3:1 a-Si: SiO_2 etch selectivity is demonstrated. This etching process can be used in applications where nanotopography is present such as single electron transistors or multigate transistors.

Keywords: Plasma Etching; Nanowire; Nanotopography; Silicon; Silicon Dioxide; Charging Effects.

1. INTRODUCTION

Novel devices and applications in nanoelectronics require both high-resolution lithography and etching processes in order to pattern increasingly small features. The next-generation devices will use a variety of new materials and geometries, together with stringent scaling requirements. A large effort has been put in the development of plasma etching of nanostructures using a variety of gases and masks [1–3]. Nevertheless, there is still a need to address the specific problem of etching silicon nanostructures over nanotopography. Such capabilities are useful for the fabrication of Single Electron Transistors (SETs) with the nanodamascene process [4], or poly-silicon multigate transistors [5].

Plasma etching processes capable of patterning these nanostructures require a high etch selectivity of the etched material with respect to both the resist and the underlying etch-stop layer, a high anisotropy, the capability to etch into nanoscale topography and etch rates that allow good control of a very thin film etch. Achieving all these conditions simultaneously is challenging. It is also common that etching processes developed for larger structures fail when applied to nanometer-sized features, because they produce defects (i.e. scallops, roughness, trenching, footing [6]) of comparable size to the actual features. These problems can be accentuated when nanostructures have to be etched on previously patterned ones.

This paper investigates the Inductively Coupled Plasma (ICP) etching of amorphous silicon (a-Si) nanos-

tructures using C_4F_8/SF_6 gases over previously patterned nanotopography in silicon dioxide (SiO_2). The first series of experiments presented in Section 2 investigates the dependence of the etch rates and selectivities with the coil power, platen power, chamber pressure and gas concentration on unpatterned samples. Section 3 presents different etching parameters on samples with both nanotrenches and nanostructures, which points out the challenges of this type of etching. Then, we demonstrate the patterning of a small 20 nm a-Si line over and perpendicular to a nanotrench (15 nm wide, 25 nm deep) in silicon dioxide with a 4.3:1 silicon:oxide etch selectivity.

2. ICP ETCHING OF PLANAR SUBSTRATES

The etching mechanisms of the C_4F_8/SF_6 plasma chemistry have been investigated for deep etching [7–12]. This section gives an investigation of the etch rates as a function of the SF_6 ratio, platen power and chamber pressure in a low power regime suitable for the patterning of shallow nanostructures. Then, the etching mechanisms of the mixed C_4F_8/SF_6 plasma in this regime are discussed. This investigation allows the optimization of the etch selectivity of a-Si relative to oxide and a-Si relative to resist. Since the etch selectivity of a-Si: SiO_2 and a-Si:resist are found to be about the same and to follow the same tendencies, only the oxide one is emphasized because of its higher importance for the suggested applications.

* Corresponding author: P.Collard@USherbrooke.ca; Tel.: +1 819-821-8000 x66204; Fax: +1 819-821-8046

2.1. Methodology

Etch rates measurements are carried out by etching unpatterned samples of a-Si, SiO₂ and electroresist (ma-N). For the SiO₂ samples, the oxide is thermally grown (1050 °C) on a p-doped silicon substrate (0.1 – 0.2 Ω m resistivity). For the a-Si samples, the silicon is grown by Low Pressure Chemical Vapor Deposition (LPCVD) at 525 °C and 300 mTorr on the SiO₂ samples previously described. They are deoxidized in diluted hydrofluoric acid (HF 49%:DI water 1:50) immediately before etching. Throughout the article the term silicon is sometimes used instead of amorphous silicon, although the etched silicon is always amorphous and undoped. The ma-N samples are SiO₂ samples spin-coated with negative electroresist ma-N 2401 from Micro Resist Technology diluted 1:1 with anisole. The resist is baked at 90 °C for 1 min and then at 100 °C for 10 min. Thicknesses of the a-Si, SiO₂ and ma-N layers are respectively 470 nm, 107 nm and 35 nm and are measured with a spectroscopic ellipsometer before and after every etch. See the online supplementary material Section 5 for additional details.

The samples are etched in a STS Multiplex Advanced Silicon Etch ICP system. They are fixed on a quartz substrate with STI Crystalbond 555HMP adhesive for proper sample thermalization during the etch. The ICP parameters investigated are the coil power P_c , the platen power P_p , the chamber pressure p , the flow ratio of SF₆ defined as $r_{\text{SF}_6} = (\text{SF}_6 \text{ flow})/(\text{total flow})$ and etch time t . The coil power is fixed to 100 W unless otherwise specified, the total gas flow is always 75 sccm and the gas used is a mixture of C₄F₈ and SF₆. The platen temperature is 20 °C. The coil and platen RF generators frequency is 13.56 MHz.

2.2. Effect of the ICP parameters on the etch rates and selectivities

ICP reactors are designed to produce high density plasmas and mainly used for deep etching and high etch rates. Thus, to control the etching of shallow nanostructures, the etch rates must rather be decreased so as to insure a good process reproducibility and avoid plasma instabilities. The reactor capability to separate the plasma generation power (coil) from the ion acceleration power (platen) allow the etch rate to be tuned via the coil power. However, it can lead to a change in the dissociation ratio of the gas species and in the etching behavior.

The etch rate measurements performed with coil powers ranging from 50 W to 600 W show that the etch rate can be tuned on a wide range of values, from 20 nm/min to 125 nm/min for amorphous silicon. More details are given in the online supplementary material (Section 6, Figure S-7 and Table S-I). The changes in the plasma (ion and radical densities) induced by this unusually low power (the usual range of this reactor is 600 – 1000 W) can be compensated by adjusting the gas ratio.

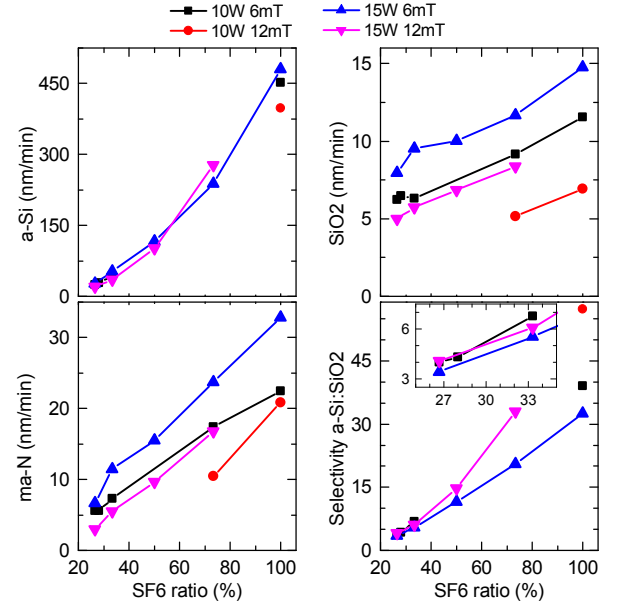


Figure 1. Etch rates of silicon, oxide and resist depending on the SF₆ ratio. The silicon:oxide etch selectivity is calculated from the etch rates. The other ICP parameters are given in the legend in the order P_p / p , where mT stands for mTorr. At very low SF₆ ratios ($\lesssim 20\%$), the passivation dominates the etching and a polymer is deposited on the sample.

A coil power of 100 W is chosen as an appropriate value and is used through the rest of the article. The chosen power is much lower than what is reported in the literature for similar systems. In comparison, Welch *et al.* [2] report powers in the range 600 – 1200 W¹ and Hung *et al.* [1] of 800 W. According to Henry [13], increasing the power in this regime reduces the etch rate of silicon, while Hung *et al.* [1] report that the etch rate is relatively insensitive to the coil power. These two statements are in disagreement with our experimental results, which show that increasing the coil power increases the etch rate. This difference could be explained by two factors. First, our regime is a low power one well suited for nanometric film etch, when the other reported work is at much higher power regimes. Second, because our ICP reactor is different, the power values used cannot be compared directly.

The effect of the gas mixture is now examined. Figure 1 shows the measured etch rates of silicon, oxide and electroresist as a function of the SF₆ ratio. The different curves in each plot are for different platen powers and chamber pressures. While the silicon etch rate variation is non-linear, the oxide and resist show linear dependencies. The etch selectivity of silicon with respect to its oxide is calculated from the etch rates and also shown in Figure 1.

¹ Data obtained through personal communication with C. C. Welch.

Silicon etching is caused by the neutral fluorine radicals released by SF_6 [9] and this process is isotropic in our regime. Accordingly, the data of Figure 1 shows that the highest silicon etch rates are obtained for pure SF_6 . When C_4F_8 is added to obtain anisotropy, the etch rate of silicon rapidly decreases. It is due to the presence of a steady-state passivation film that protects the silicon from being etched by fluorine, which has to diffuse through it to react with silicon [10]. The steep slope indicates that too much passivation by C_4F_8 will highly degrade the a-Si:SiO₂ and ma-N:SiO₂ etch selectivity. It is important to note that SF_6 ratios of 20 to 40 % are needed to obtain significant anisotropy. The optimal values reported in the literature [1, 2] depend on the ICP parameters. Our results using a variety of ratios are presented in the following section and in the online supplementary material Figure S-8.

For pure C_4F_8 , a polytetrafluoroethylene (PTFE)-like polymer is deposited on the surface. Our data in the online supplementary material Table S-II shows that the deposition rate of this polymer is slightly enhanced by the platen power. This suggests that the passivation mechanism has an ionic component.

It is clear from Figure 1 that pure fluorine also etches the oxide. However, the etch rate reduction caused by the addition of C_4F_8 is much less dramatic than in the a-Si case. In addition, it is seen that the SiO₂ curve has a smaller slope than the ma-N one. This suggests that CF_x components from C_4F_8 participate in the chemical etching reaction, an observation also reported in the literature [9]. Carbon has a strong bond to oxygen and is abundant in the passivation film at the surface, whereas fluorine has to diffuse through the film. When carbon binds to oxygen to produce CO_2 , more dangling bonds are left for fluorine to react with silicon. This process requires ionic bombardment to provide the activation energy [14].

The effect of the platen power is now examined. Figure 2 shows the measured etch rates as a function of the platen power. The latter causes the ions to be accelerated towards the sample. For silicon etching in pure SF_6 , the relatively small dependence of the silicon etch rate on platen power indicates that ions do not limit the etch rate (although they may play an activation role) [11]. The Scanning Electron Microscope (SEM) inspection of etch profiles revealing isotropic etching (see online supplementary material Figure S-8 for images) reinforces this conclusion, because isotropy is typical of etching by neutral radicals. The relative insensitivity of the silicon etch rate to the platen power is not changed by the addition of C_4F_8 . However, anisotropy is observed due to the passivation of the sidewalls. The etch rates of SiO₂ and ma-N are dependent on the platen power, implying that their etching mechanisms are strongly ion-enhanced.

Figure 3 plots the etch rates of silicon, oxide and resist as a function of the chamber pressure. Its effect is similar on the etch rates as the platen power one, namely that it affects mostly the oxide and the resist. Lowering the

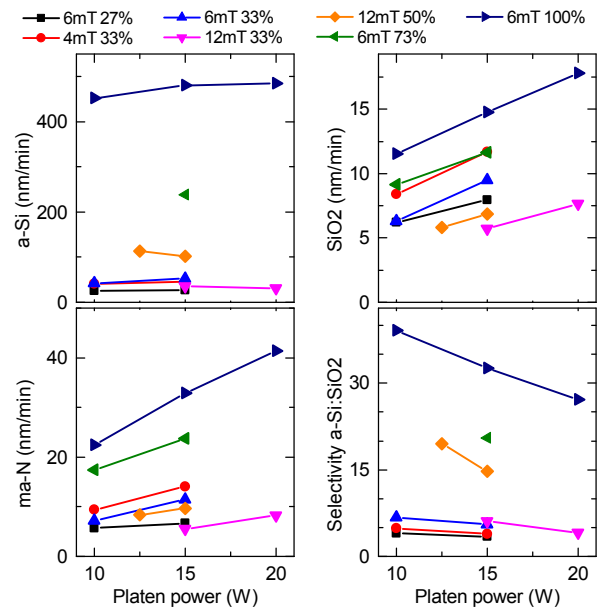


Figure 2. Etch rates of silicon, oxide and resist depending on the platen power. The silicon:oxide etch selectivity is calculated from the etch rates. The other ICP parameters are given in the legend in the order p / r_{SF_6} , where mT stands for mTorr.

pressure is known to increase the flux and energy of the ions due to the longer mean free path and a modification of the sheath [9], but in different proportions than the platen power does. The silicon:oxide etch selectivity is also plotted in Figure 3.

3. ICP ETCHING OF NANOSTRUCTURES

In this section, results related to nanostructures and nanotrenches are presented. The previous investigation of the dependence of the silicon:oxide and silicon:resist etch selectivity on the ICP parameters allows the process to be nearly optimal concerning selectivity, while exploring the impact of these parameters on other etching characteristics such as anisotropy, Aspect Ratio Dependent Etch rate (ARDE) or footing [6]. We discuss the factors that influence the vertical profile of the etched structures and the capacity of the process to etch into nanotrenches. Finally, we present a working process and discuss the trade-offs of the different parameters.

3.1. Methodology

Three different types of samples are used to investigate the behavior of the process on both nanotrenches and nanostructures. Type A samples are patterned for a SET application (see Figures 4b and 4c). They have silicon nanowires patterned over trenches in oxide. Type B samples are thick a-Si samples patterned with negative

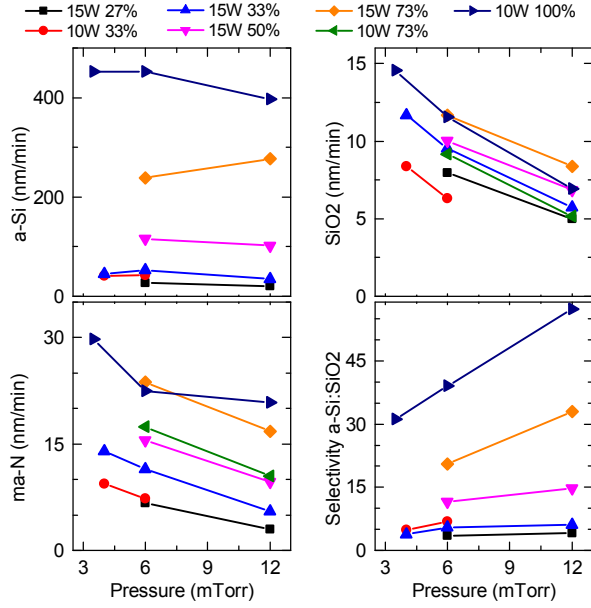


Figure 3. Etch rates of silicon, oxide and resist depending on the chamber pressure. The silicon:oxide etch selectivity is calculated from the etch rates. The other ICP parameters are given in the legend in the order P_p / r_{SF_6} .

ma-N resist test structures. Type C samples are thick a-Si samples patterned with positive ZEP resist. In the following paragraphs, we detail the fabrication parameters of the samples.

Type A samples have a 107 nm thermally grown SiO₂ layer. The oxide is plasma etched with a mask of positive ZEP electroresist to form 15 – 25 nm wide and 20 nm deep trenches in the oxide using the process developed by Guilmain *et al.* [15]. The trenches are then filled by a 40 nm thick a-Si LPCVD layer. A 35 nm thick ma-N mask is used for the a-Si nanowires that will be etched using the C₄F₈/SF₆ plasma. The resist and polymer residue are ashed in an oxygen plasma after the etch (type A only).

Type B samples have a thick 470 nm a-Si layer over the 107 nm SiO₂ samples prepared as described in the previous section. A ma-N mask is used for the a-Si nanostructures.

Type C samples are similar to type B, but are patterned with positive ZEP resist instead. The Zeon Corp. ZEP 520A resist is diluted 2.4:1 (weight) with anisole and its thickness is 90 nm. All three types of samples are de-oxidized in diluted HF with the patterned resist prior to the etch.

For the type A samples, the etch time t is calculated as following. Knowing the etch rates of planar films, the etch time of the native oxide, a-Si bulk film and trench depth is calculated and added. The total time is then multiplied by an overetch factor f_{overetch} chosen between 1.10 and 1.25. For the type B and C samples, the etch time is chosen to create either structures or trenches 30 – 100 nm deep.

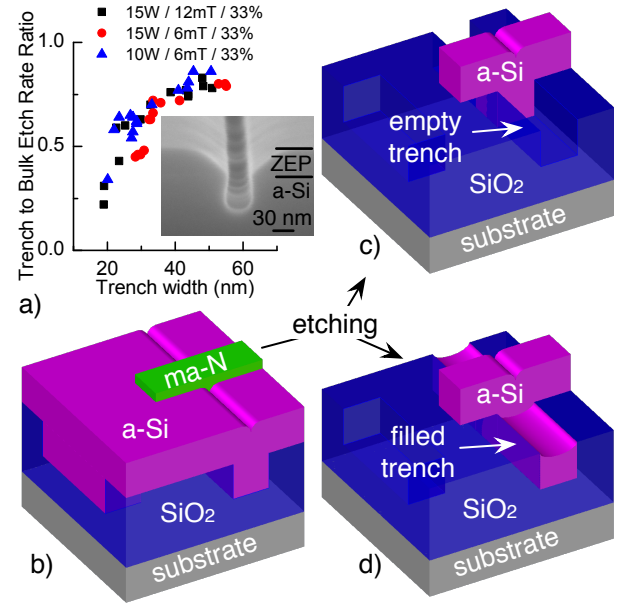


Figure 4. a) Etch rate ratio between narrow trenches in a-Si and wide 10 μm trenches (type C samples). The ICP parameters are given in the legend in the order $P_p / p / r_{SF_6}$. In this test, trenches are etched in a-Si using ZEP electroresist as a mask (SEM micrograph inset). All the tested parameters seem to have the same behavior when etching in narrow ZEP and a-Si trenches. b) Schematic of type A samples before etching. c) Schematic of type A samples after etching. This is the target structure. d) For some parameters, the ICP process is unable to etch the a-Si inside the nanotrench, as illustrated on the schematic.

3.2. Etching in small nanotrenches

A reduction of the etch rate in small trenches depending on their aspect ratio, a phenomenon known as ARDE, is expected due to microloading. In Figure 4a, the etch rate of a-Si trenches defined by an opening in positive ZEP resist is measured and compared to the rate of a 10 μm opening considered to be the bulk etch rate. Three processes are tested with different pressures and platen powers, but same SF₆ ratios, to check for the best parameters to reduce ARDE. The data shows that there is no significant difference between the three.

Similar parameters are then tested on type A samples, which are the target structures illustrated in Figure 4c. In Figure 5, SEM images of the etched nanostructures are shown. We see that in Figures 5a and 5b the oxide trench is not empty, while the ones of Figures 5c and 5d are. Hence, the same three conditions used for the test of Figure 4a are not equivalent in this situation. Other structures etched with 25 % overetch show the same results. Comparing Figures 5a with 5c, and 5b with 5d, we find that the successful conditions are the 6 mTorr pressure ones, a result that could not be anticipated from the test of Figure 4a. Other combinations of parameters were tested and confirm these results. In particular, a

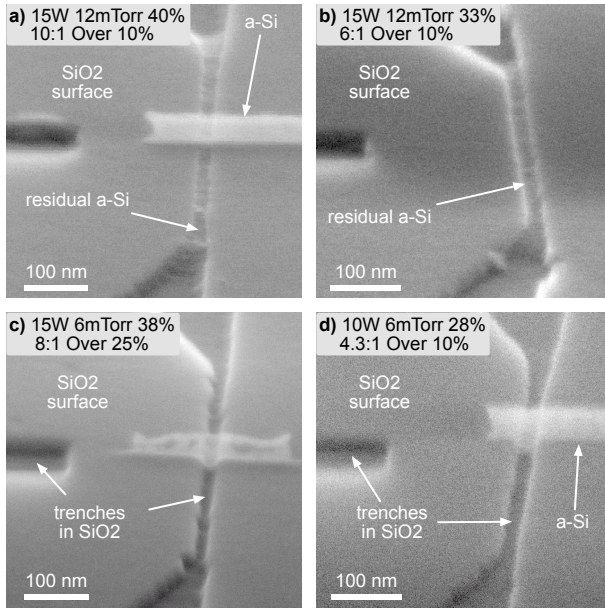


Figure 5. Effect of different etch parameters on the etching of silicon inside small (< 25 nm) trenches in oxide (type A samples). The parameters are given in the order $P_p / p / r_{SF_6} / \text{a-Si:SiO}_2$ etch selectivity / overetch. a) and b) resemble the schematic of Figure 4d. A good process is presented in d), where we see that the a-Si nanowire goes down inside the trench like in Figure 4c.

10 W / 6 mTorr / 33 % / 7:1 / Over 10 % process having about the same etch selectivity and physical etching as Figure 5b (because their oxide and resist etch rates are similar and are mostly of ionic origin) was tested, yet only the 6 mTorr process clears the a-Si in the trench. All the nanowires show undercutting because of the high SF_6 ratio, except for the one in Figure 5d. This last process demonstrates a good vertical profile and a trench clear of silicon, which is the intended result.

3.3. Anisotropy and surface effects

Anisotropy is obtained by passivating the sidewalls with a fluorocarbon polymer. In Section 2, we showed that C_4F_8 provides this passivation at the expense of the silicon:oxide etch selectivity. Therefore, tuning the SF_6 ratio is important for both anisotropy and etch selectivity.

In Figure 6a, type A (right) and type B (left) samples are etched and imaged with an SEM at a low 15° tilt angle. In the left image, there is no stop layer, so the surface exposed to the plasma is a-Si. In the right image, the etch is carried out over topography: the etch stops on the oxide layer (surface is SiO_2). Because of the need to etch into the nanotrench, almost 50 % of the etch is carried out while the oxide surface is exposed to the plasma. The processes are underpassivated, leading to some undercutting of the features. Nevertheless, the

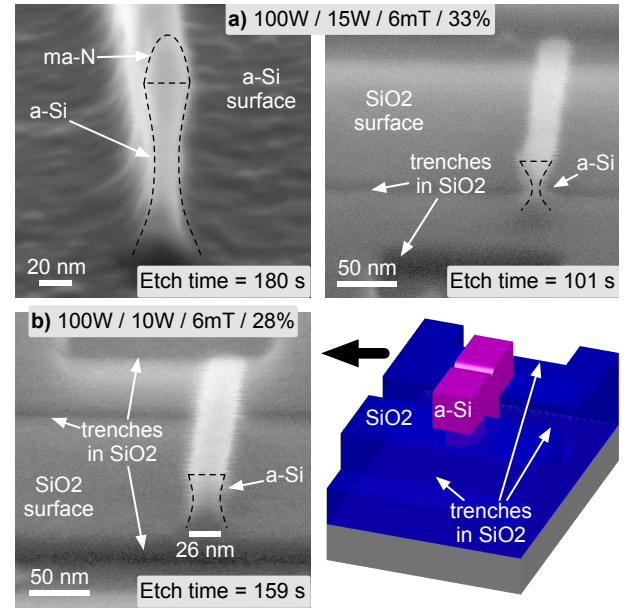


Figure 6. SEM sideview of an a-Si nanowire for different etch-stop layers. a) In the left image, there is no stop layer (type B samples, surface is a-Si). In the right image, the etch is carried out over topography: the etch stops on the oxide layer (type A samples, surface is SiO_2). The silicon nanowire is more severely undercut in the presence of the oxide stop layer. b) Good vertical profile is realized by using a lower SF_6 ratio.

structure on the right is much more undercut than the one on the left, even if the etch time is smaller. Most of the right sample structures were in fact completely collapsed or about to. This phenomenon was observed with other sets of parameters as well.

The authors in references [1, 2] report that SF_6 ratios of 30 – 35 % produce vertical sidewalls and that the optimal value for verticality is pressure-dependent. Although in our work such values also produced near-vertical sidewalls when using type B samples, lower 26 – 28 % values were needed for type A samples because of the oxide layer, as shown in Figure 6b. According to Figure 1, this reduces the a-Si: SiO_2 etch selectivity by about a third. Since it was previously established that the pressure is the key to clearing the silicon from the nanotrenches, the platen power can be lowered from 15 to 10 W with no impact on the silicon nanotrench etching. According to Figure 2, a lower platen power allows to compensate partly for the drop in selectivity caused by the lower SF_6 ratio. Hence, our work shows that the optimal SF_6 ratio also depends on the presence or absence of an oxide etch-stop layer and provides a method for optimizing the processing conditions. See the online supplementary material Table S-I for a comparison of the etching parameters for the two different scenarios.

3.4. Discussion on the surface charging effects

We demonstrated that the presence of the oxide surface increases the undercut on standing a-Si nanostructures (Figure 6) and that it inhibits the etching into trenches when using a high pressure process (Figure 5). A possible explanation for these results is that the oxide surface charges positively when exposed to the plasma. Charging effects can cause sidewalls to be undercut, provoke footing and can slow the etching of surfaces [16, 17]. In our case, the effect observed has to be related to the oxide surface, because any effect caused by the nanostructure would always be present and thus unnoticed. A positive charge on the oxide would deflect the ions towards the sidewalls, causing etching of the passivation layer and an undercut as observed. It could also repel ions with low energy, preventing them from clearing the passivation layer at the surface of the trench.

The results show that the pressure is the parameter that has the most impact on the nanotrench etching, and similar results are reported by Park *et al.* [17]. We suggest that a lower pressure changes the energy distribution of the ions towards higher energies, while changing the amount of charge build-up on the surface, in a way that is favorable to overcome the charging effects. This would be consistent with the work of Park *et al.* [17].

We also see that using a higher platen power does not enhance the etching into the oxide trenches, because processes with $P_p = 15$ W work only at low pressures. Moreover, high platen powers degrade the a-Si:SiO₂ etch selectivity. Also, in the online supplementary material (Table S-II), we show using pure C₄F₈ that increasing the platen power increases the deposition rate of the fluorocarbon polymer. This suggests that the passivation layer is itself charged because of the ionic contribution.

We also exclude that the problem observed is an effect of the a-Si:SiO₂ etch selectivity. In Figure 5, we see no correlation between etch selectivity (4:1 to 10:1) and the capacity to etch inside the trenches. Nevertheless, we observed in other experiments that using an extremely high SF₆ ratio (73 %) enables the trench etching at high pressures. In this ratio regime, the etch selectivity has a high 34:1 value but the etching is isotropic. We suggest that in this extreme case, the steady-state passivation

layer on the surface is not sufficient to prevent the neutral fluorine from etching the trench, even in the case of charge build-up.

Experiments with a precise monitoring of the density and energy of the ions, combined with simulation, would be needed to confirm these predictions, but are beyond the scope of this work.

4. CONCLUSION

ICP etching of amorphous silicon nanostructures over nanotopography has been realized using C₄F₈/SF₆ continuous plasma. Our results show that the coil power can be used to tune the etch rate to allow reproducible etching of 40 nm thin films. Using a power of 100 W, we have then demonstrated how the etch rates and selectivities depend on the SF₆ ratio, platen power and chamber pressure. These results give insights on the microscopic etching mechanisms. Our processes have been applied to various types of nanopatterned samples. We have observed that the amount of passivation by C₄F₈ needed to obtain vertical sidewalls is higher in the presence of an oxide etch-stop layer. To etch the silicon inside the oxide nanotrenches, it is necessary to use a low pressure of 6 mTorr. While a 12 mTorr pressure or higher allows a better a-Si:SiO₂ etch selectivity, the etch stops when the oxide surface is exposed, leaving the trench incompletely etched, even with a severe overetch. It has been argued that the surface-dependent vertical profile and the nanotrench etching can both be explained by charging effects. Finally, we have demonstrated a process to produce highly conformable 20 nm a-Si nanowires that cross 15 nm trenches in oxide with vertical sidewalls and an a-Si:SiO₂ etch selectivity of 4.3:1 suitable for applications with nanotopography, such as multigate transistors or SETs.

ACKNOWLEDGMENTS

The authors thank C. Sarra-Bournet for fruitful discussions concerning this work and C. Bureau-Oxton for the careful reading of the manuscript. This work was supported by NSERC, FRQNT, NanoQuébec and CIFAR.

-
- [1] Y.-J. Hung, S.-L. Lee, B. J. Thibeault, and L. A. Coldren, *IEEE Journal of Selected Topics in Quantum Electronics* **17**, 869 (2011).
 - [2] C. C. Welch, A. L. Goodyear, T. Wahlbrink, M. C. Lemme, and T. Mollenhauer, *Microelectronic Engineering* **83**, 1170 (2006), [Link].
 - [3] M. D. Henry, M. J. Shearn, B. Chhim, and A. Scherer, *Nanotechnology* **21**, 245303 (2010), [Link].
 - [4] C. Dubuc, J. Beauvais, and D. Drouin, *IEEE Transactions on Nanotechnology* **7**, 68 (2008).
 - [5] I. Ferain, C. A. Colinge, and J.-P. Colinge, *Nature* **479**, 310 (2011), [Link].
 - [6] S. Franssila, *Introduction to Microfabrication* (Wiley, 2010), 2nd ed.
 - [7] R. A. H. Heinecke, *Solid-State Electronics* **18**, 1146 (1975), [Link].
 - [8] R. d'Agostino and D. L. Flamm, *Journal of Applied Physics* **52**, 162 (1981), [Link].
 - [9] D. L. Flamm and V. M. Donnelly, *Plasma Chemistry and Plasma Processing* **1**, 317 (1981), [Link].

- [10] N. R. Rueger, J. J. Beulens, M. Schaepkens, M. F. Doemling, J. M. Mirza, T. E. F. M. Standaert, and G. S. Oehrlein, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **15**, 1881 (1997), [\[Link\]](#).
- [11] J.-H. Min, G.-R. Lee, J. kwan Lee, S. H. Moon, and C.-K. Kim, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* **22**, 893 (2004), [\[Link\]](#).
- [12] S. Chen, Y. Lin, J. Wu, L. Horng, and C. Cheng, *Microsystem Technologies* **13**, 465 (2007), [\[Link\]](#).
- [13] M. D. Henry, Ph.D. thesis, California Institute of Technology, Pasadena, California (USA) (2010).
- [14] M. A. Lieberman and A. J. Lichtenberg, *Principles of Plasma Discharges and Materials Processing* (Wiley, 2005), 2nd ed.
- [15] M. Guilmain, A. Jaouad, S. Ecoffey, and D. Drouin, *Microelectronic Engineering* **88**, 2505 (2011), [\[Link\]](#).
- [16] J. C. Arnold and H. H. Sawin, *Journal of Applied Physics* **70**, 5314 (1991), [\[Link\]](#).
- [17] H. S. Park, S. J. Kim, Y. Q. Wu, and J. K. Lee, *IEEE Transactions on Plasma Science* **31**, 703 (2003).

Online Supplementary Material for: Inductively Coupled Plasma etching of amorphous silicon nanostructures over nanotopography using C_4F_8/SF_6 chemistry

5. DETAILS ON ETCH RATES MEASUREMENTS

To perform the etch rate measurements, the thicknesses of the a-Si, SiO_2 and ma-N layers are measured with a spectroscopic ellipsometer before and after every etch. The etched thickness is then divided by the etch time to compute the etch rates. The etch selectivity is defined as the etch rate ratio of two materials.

The measured ellipsometric thicknesses are consistent with profilometric measurements. The a-Si layer includes a native oxide layer. The refractive index n and absorption coefficient k of the ellipsometric model of the a-Si and ma-N layers is fitted along with the thickness every time. The n and k did not change significantly after the etch. All other layers have a fixed n and k value. Some roughness and fluorocarbon etch residue is seen in the model as a higher native oxide thickness after the etch, which is typically 1–2.5 nm. All fits are good and fitting error is low.

The measurements are accurate within one nanometer and the etched thicknesses range from 25 to 400 nm depending on the etch rate. This gives a relative uncertainty of 0.5 % to 8 % in the worst case. The variability in the etch rate measurements is also due to the etch rate increasing slightly over time. The etch times range from 45 s to 120 s. For instance, the data point at 33 % SF_6 of the 15 W / 6 mTorr data set of Figure 1 has an etch time of 120 s, whereas the others have a 60 s one. This point is off with the others by 15 % because the etch rate increased during the etch. Despite these measurement imprecisions, it's the dependency of the etch rates with the ICP parameters that's important. Having extremely precise values is of secondary importance since they would be different on a different reactor. Error bars do not appear in the article because they make the graphs harder to read.

6. EFFECT OF THE COIL POWER

In this section, more data is presented on the effect of the coil power on the etch rates. Since the main objective of the article is to investigate the etching of nanostructures, the effect of the coil power has not been studied thoroughly. It is sufficient to find a regime where the total etch time allows the reproducible etching of a very thin film (about 40 nm). The consistency of the results presented in the article is a strong indication that the plasma is stable even in the low power regime used (100 W) and can be used to etch nanostructures reliably.

Using the coil power, the etch rate of a-Si can be varied from about 20 to 125 nm/min. These values are taken from different etching processes used throughout the pa-

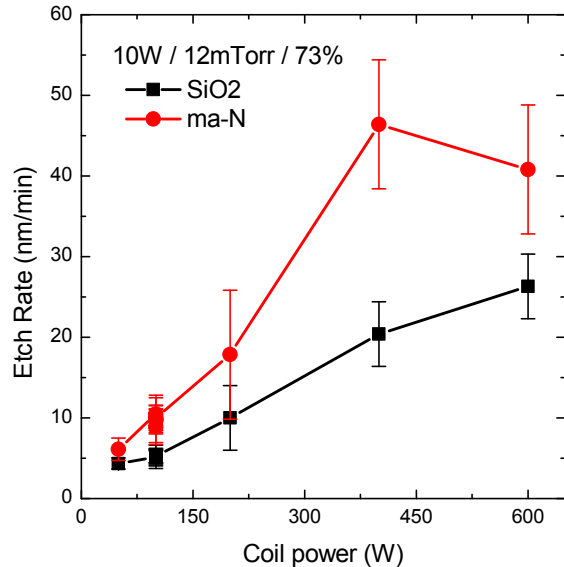


Figure S-7. Etch rate of silicon dioxide and ma-N resist depending on the coil power. The other ICP parameters are given in the legend in the order $P_p / p / r_{SF_6}$.

per with a fixed 26–28 % SF_6 ratio (but with no specific chamber pressure or platen power). This gas ratio allows a high anisotropy and almost vertical sidewalls. The conclusion of all the tests conducted is that the coil power has a high impact on the etch rates, while the other properties are only slightly affected. This impact has not been studied quantitatively.

As an exemple of such a coil power effect, Figure S-7 plots the oxide and resist etch rates as a function of the coil power. With 73 % SF_6 , this process is nearly isotropic. The short 15–45 s etch times explain the high error bars on the data. The erratic point on the ma-N curve at 400 W is due to the etch time of 15 s, which is too short to allow a good plasma stability. The a-Si data set is missing because the a-Si thin films used were too thin (40 nm, which is thinner than those of the data sets of the article) and the a-Si etch rates too fast, meaning that they were completely etched.

In Table S-I, we give details about two similar processes at different coil powers. The first one is tuned for an application that doesn't require a lot of overetching after an oxide surface is reached. The second is tuned for an application where nanotopography is involved and significant overetching is required, like the one of Figure 4. Because a lower pressure is necessary, the etch selectivity is reduced by almost a factor of 2.

Table S-I. Comparison between achievable selectivities when etching bulk a-Si and over topography in oxide. The topography requirement cost almost a factor of 2 in etch selectivity because of the lower pressure required. Note that it is not the lower coil power used that causes this loss in etch selectivity.

Process	Normal	Over topography
P_c (W)	600	100
P_p (W)	10	10
p (mTorr)	12	6
SF ₆ ratio (%)	26.7	28.0
a-Si (nm/min)	125	27.9
a-Si:SiO ₂	7.5:1	4.3:1

Table S-II. Fluorocarbon passivation layer deposition depending on platen power. The other ICP parameters are $P_c = 100$ W, $p = 12$ mTorr, C₄F₈ flow = 20 sccm.

Platen Power (W)	Deposition Rate (nm/min)
20	26
50	32

7. PASSIVATION RATE

In Table S-II, the deposition rate of the fluorocarbon polymer deposited by C₄F₈ on a SiO₂ sample is measured. The passivation rate is enhanced by the platen power and hence has an ionic component.

8. EFFECT OF THE SF₆ RATIO ON THE VERTICAL PROFILES

In Figure S-8, the left column provides data showing the undercut of nanostructures depending on the SF₆ ratio. The etching is isotropic at 100 % SF₆ and perfectly anisotropic at 27 % SF₆. This last setting allows the fabrication of small 11 nm nanowires. In the right column, trenches in silicon dioxide are cleared of their silicon filling, a characteristic that is required when patterning structures over topography.

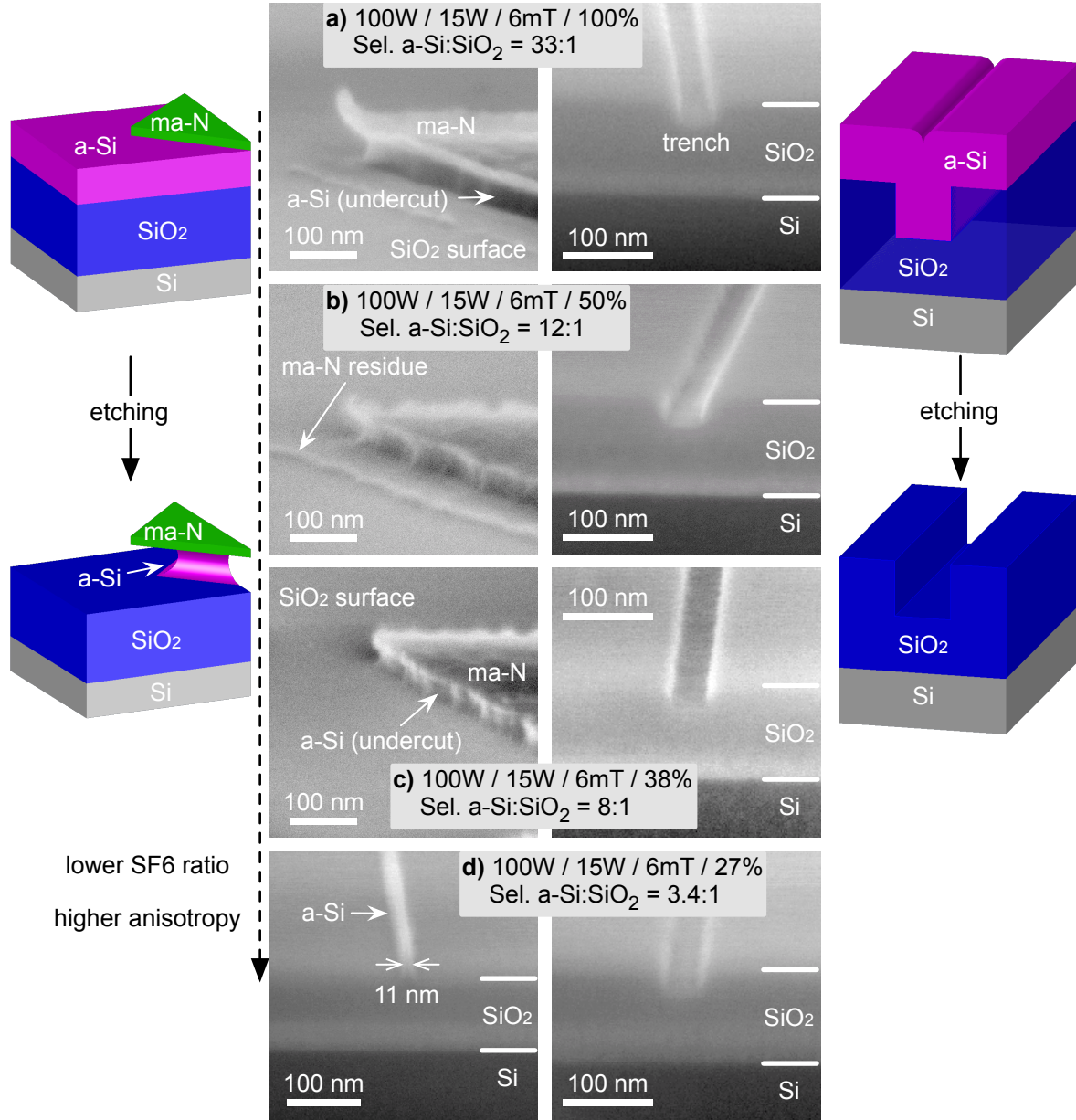


Figure S-8. Etch profile of type A samples over a wide range of SF_6 ratios. Left column: 40 nm thick a-Si structures. Right column: trenches in oxide. The parameters are given in the order $P_c / P_p / p / r_{\text{SF}_6}$, where mT stands for mTorr. Trenches are about 40 nm wide and 26 nm deep. In a), b) and c), the a-Si structures are clearly undercut, showing too low or no passivation. In d), an 11 nm wide nanowire shows a vertical profile at the expense of the a-Si:SiO₂ etch selectivity. In all images the trenches in oxide are clear of silicon, an important property for etching over topography.